IN THE SPECIFICATION

Please replace the first paragraph on page 10 with the following paragraph:

Another advantage of this particular architecture is the ability to cascade or line up all the channels together. In one embodiment of the present invention the back side or memory array side has individual first in first out (FIFO) channels. Each individual channel at the receive parallel output forwards the signals through an elasticity buffer. The elasticity buffer facilitates correction of phase differences between channels if there is a phase skew (e.g., of the channel of up to one byte time). For example, data may be coming in one two different channels and become skewed in time due to the length of the serial cable. In one exemplary implementation, even though the information is configured as a parallel line up of the serial data information, when it is translated to the parallel side it may be skewed by plus or minus one byte. The elasticity buffer allows the data to be put in temporary storage while it is writing data with the serial cover clock. For example, the data is actually lined up while being read from the 250 MHz local clock side. In one embodiment of the present invention the synchronization symbol is a K28.5 signal that prevents data from being forwards until data is appropriately lined up in each parallel channel (e.g., four channels). In one embodiment, the present invention includes an elasticity buffer as described in "Circuitry, Architecture, and Method (s) for Synchronizing Data" (U.S. Patent 6,594,325~~Application NO. 09/392,042~~), incorporated herein by this reference.

Please replace the second paragraph on page 11 with the following paragraph:

In one embodiment of the present invention, the information configuration core includes a transmit channel comprising a phase aligner, encoder and serializer and each receive channel includes a deserializer, framer, decoder and an elasticity buffer. Figure 7 is a block diagram of one exemplary implementation of an information configuration core including transmit channel 250 and receive channel 270. Transmit channel 250 includes phase aligner 251, encoder 252 and serializer253. Receive channel 270 includes deserializer 271, framer 272, decoder 273 and elasticity buffer 274. The phase aligner for aligns signals forwarded from said memory array interface, the encoder encodes the signals and the serializer serializes signals received from the memory array interface. The deserializer deserializes information received from the system interface, the framer frames the information, a decoder decodes the information, and the elasticity buffer buffers the information received from said system interface.

Please replace the first paragraph on page 16 with the following paragraph:

In step 530 information is configured in proper alignment for communication between serial system controller signals and parallel memory array signals. Configuring information includes coordination for conveyance of serial signals at a first relatively fast rate to a system memory controller and conveyance of parallel signals at a second relatively slow rate to a memory array. In one embodiment of the present invention, information is communicated via an information configuration core. In one exemplary implementation of the present invention the signals on a transmit channel are phase aligned, encoded and serialized. Figure 6A is a flow chart of exemplary

transmit channel 610 in which signals are phase aligned in step 611, encoded in step 612, serialized in step 613. The signals on a receive channel are deserialized, framed, decoded and buffered (e.g. be an elasticity buffer). Figure 6B is a flow chart of exemplary receive channel 620 in which signals are deserialized in step 621, framed in step 622, decoded in step 623 and buffered in step 624.

Please add the following paragraphs at the end of the brief description of the drawings on page 7.

Figure 6A is a flow chart of exemplary transmit channel in accordance with one embodiment of the present invention.

Figure 6B is a flow chart of exemplary receive channel in accordance with one embodiment of the present invention.

Figure 7 is a block diagram of an information configuration core in accordance with one embodiment of the present invention.